EE 330 Fall 2024
Homework 6 Solutions

Problem 1 : Assume a resistor has a resistance of $1k\Omega$ at $T = 300°k$. If the TCR of this resistor is constant of value 2000ppm/oc, what will be the resistance at $T = 350° k$?

Solution

$$R(T_2) = R(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right] =$$

$$R(350°k) = R(300°k)\left[1 + (350-300)\frac{2000}{10^6}\right]$$

$$R(350°k) = 1000\left[1 + \left(50 \times \frac{2000}{10^6}\right)\right] = 1100\,\Omega = 1.1k\Omega$$

2.

We got the value of resistivity based on the doping density.

Doping density → $5 \times 10^{14}\ cm^{-3}$

Resistivity → $9.045\ \Omega\text{-cm}$

$$R = \frac{\rho L}{WH} = \frac{9.045 \times 0.2}{0.015 \times 0.005} = 24.12k\Omega$$

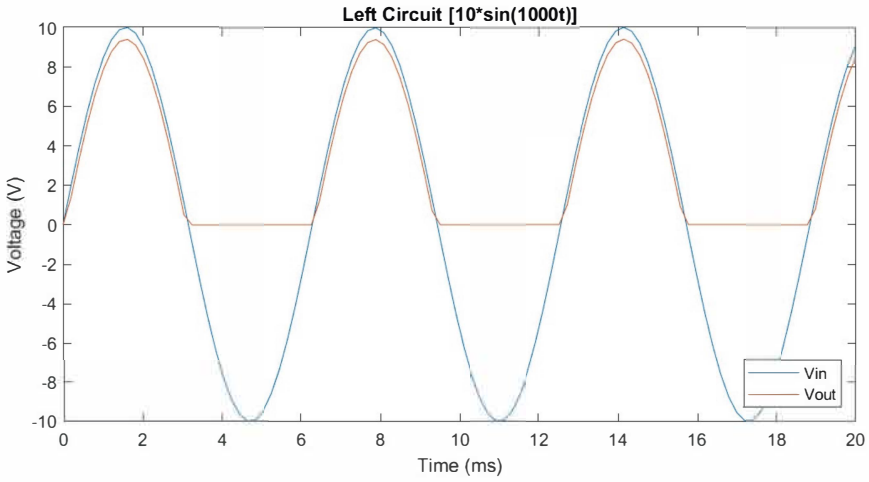
Problem 3

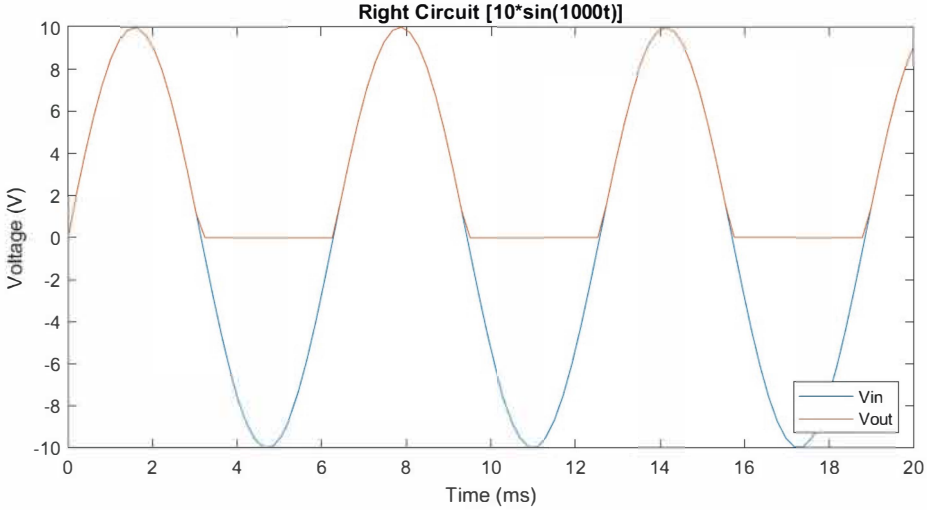
A) Left: if $V_{in} > 0.6$ then diode on else diode off, $v_{out} = 0$

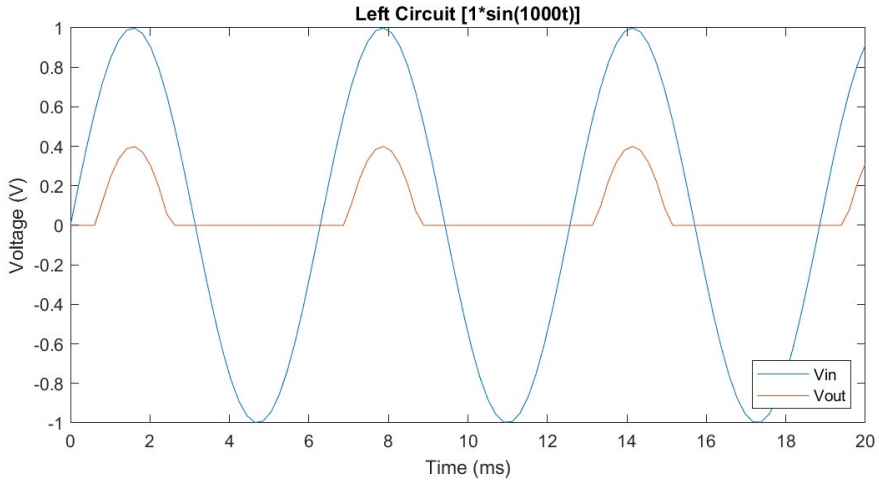
$$V_{out} = \begin{cases} 0 & V_{in} < 0.6 \\ V_{in} - 0.6 & V_{in} \geq 0.6 \end{cases}$$

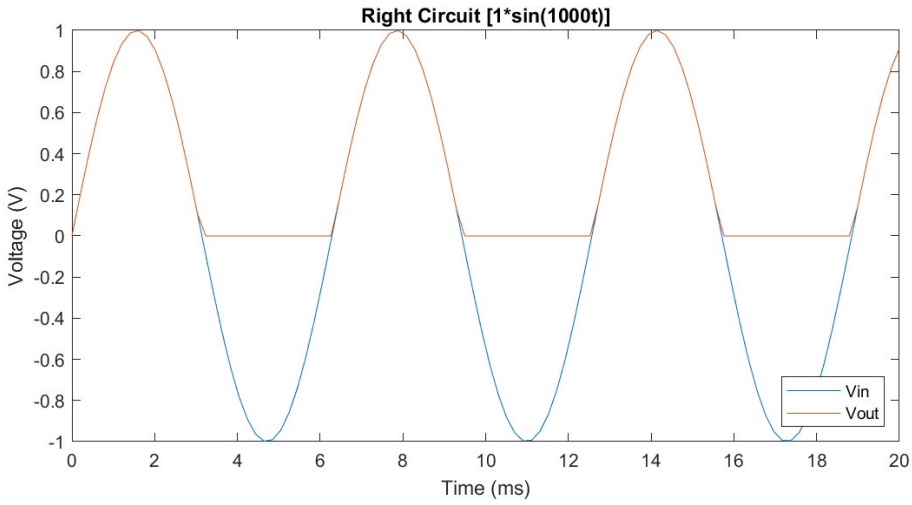
Right: if V_{out} neg then I_R is up and not possible with diode, so only positive voltages are passed

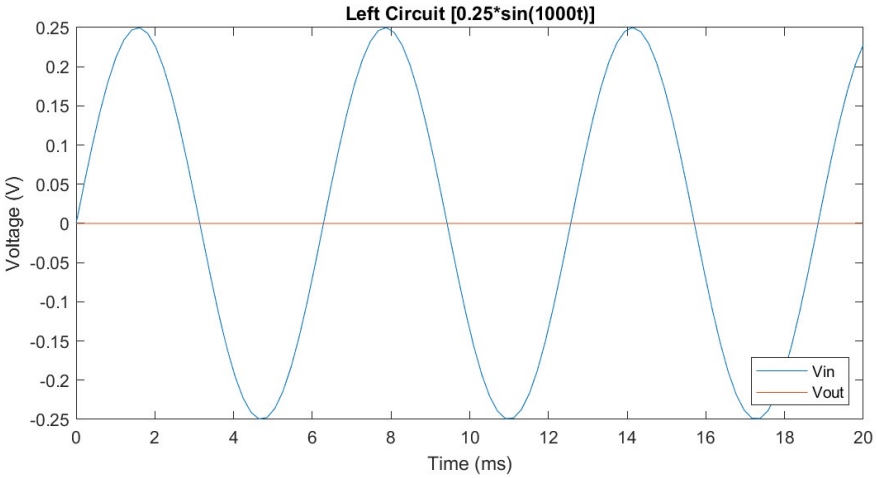
$$V_{out} = \begin{cases} 0 & V_{in} < 0 \\ V_{in} & V_{in} \geq 0 \end{cases}$$

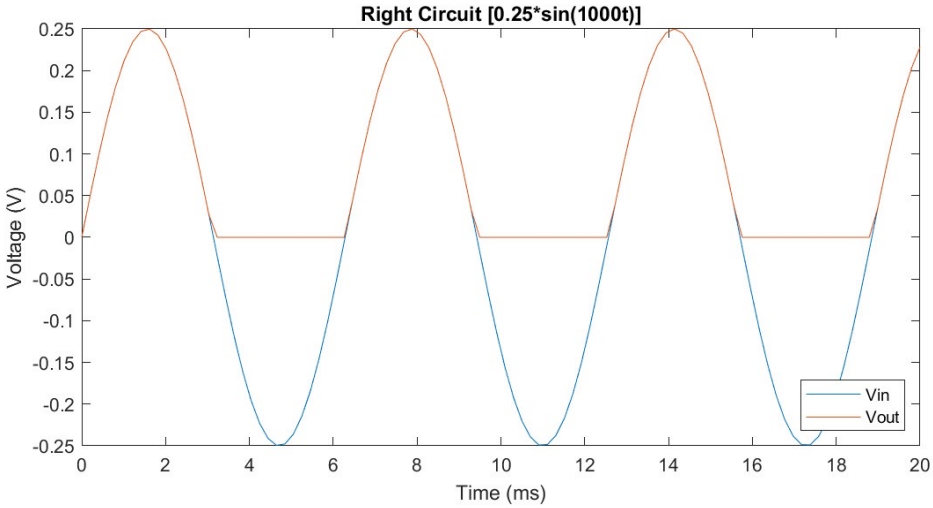





Left Circuit [1*sin(1000t)]
Voltage (V)
Time (ms)
Vin
Vout


Right Circuit [1*sin(1000t)]
Voltage (V)
Time (ms)
Vin
Vout


Left Circuit [0.25*sin(1000t)]
Voltage (V)
Time (ms)
Vin
Vout


Right Circuit [0.25*sin(1000t)]
Voltage (V)
Time (ms)
Vin
Vout

Problem 4 (a)

Using voltage divider, $V_{out} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_{in}$

3dB frequency = Cut off frequency = $f_c = 10MHz$

$\rightarrow f_c = \frac{1}{2\pi RC}$

$\rightarrow C = \frac{1}{2\pi R f_c} = \frac{1}{2\pi \times 10 \times 10^3 \times 10 \times 10^6} = 1.592 \times 10^{-12} = 1.592pF$

$\rightarrow$ Using $R(T_2) = R(T_1)\left[1 + (T_2 - T_1)\frac{2300}{10^6}\right]$

$C(T_2) = C(T_1)\left[1 + (T_2 - T_1)\frac{1000}{10^6}\right]$

the temperature value pairs for each resistor can be found as

$\rightarrow$ At 273K, $R = 10K\Omega$, $C = 1.592pF$ and the 3dB frequency = 10MHz

$\rightarrow$ At 350K, $R = 11.771K\Omega$, $C = 1.715pF$ and 3dB frequency = 7.88MHz

so the graphs will look as shown below with the 3dB frequency or cut off frequency as calculated above.

(b)

% change in 3dB frequency $= \frac{10MHz - 7.88MHz}{10MHz} \times 100\%$

$= 21.2\%$

5.

P5) What is the range in the diode current?

$I_D = J_s A \, e^{\frac{V_D}{nV_t}}$ $\quad V_D = 0.5V$ or 0.6

$J_s = 10^{-15} A/u^2$ $\quad V_t = 26mV$

$A = 50u^2$ $\quad n = 1$

0.5 V

$I_D = 10^{-15} \frac{A}{u^2} \cdot 50u^2 \; e^{\frac{0.5V}{26mV}}$

$I_D = 11.241 uA$

0.6V

$I_D = 10^{-15} A/u^2 \cdot 50u^2 \; e^{\frac{0.6V}{26mV}}$

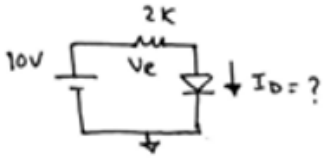
$I_D = 526.199 uA$

The range in the diode current is between

$11.241uA \sim 526.199uA$

P6.) Determine the current I_D. $V_x = 10V$ $\quad A = 200u^2$

$J_s = 10^{-15} A/u^2$ $\quad V_t = 26mV$



$V_x = I_D \cdot R + V_D$ $\quad V_D = 0.6V$

$\Rightarrow 10V = I_D \cdot 2K + 0.6V$

$I_D = \frac{10V - 0.6V}{2K} = 4.7mA$

Diode is "on"

$I_D = 4.7mA > 0$

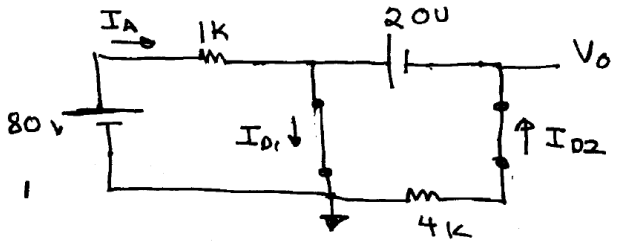
7). Since V_x is much smaller, it can be shown that the simplified diode models will not be good enough to accurately predict I_D so must use diode equation

$$520mV = I_D(2k) + V_D$$
$$I_D = J_s A\, e^{\frac{V_D}{nV_t}}$$

} eliminate V_D $\quad 520mV = 2kI_D + nV_t \ln\left(\frac{I_D}{J_s A}\right)$

with $n=1$, $V_t = 25mV$ and $J_s A = 2E-14$, solving iteratively for I_D we obtain $I_D = 26.5\mu A$

8) For circuit on left Guess D1 and D2 ON.



To verify guess, must show $I_{D1} > 0$ & $I_{D2} > 0$

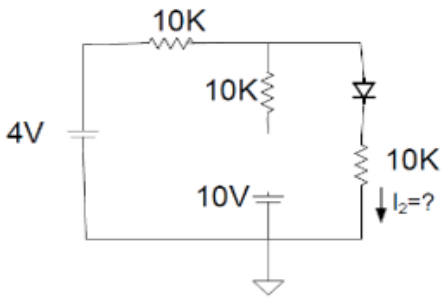
solving, obtain $V_o = -20V$. must now verify

$$I_{D2} = \frac{20V}{4k} = 5mA \qquad I_{D1} = I_A + I_{D2} = \frac{80V}{1k} + 5mA = 85mA$$

thus $I_{D1} > 0$ & $I_{D2} > 0$ so $V_o = -20V$ solution is valid

For the right circuit:

I will start by assuming the middle diode is off, and the rightmost diode is on. This guess is made on the assumption that the location of the 10V source relative to the 4V source will cause currents to flow in the wrong directions. This allows us to treat the middle diode as an open circuit, giving us the following diagram.



As the 10V source drives an open circuit and the 10kΩ resistor ends at an open circuit, we can neglect them. Using KVL, we can find the current through the loop using the following equation:

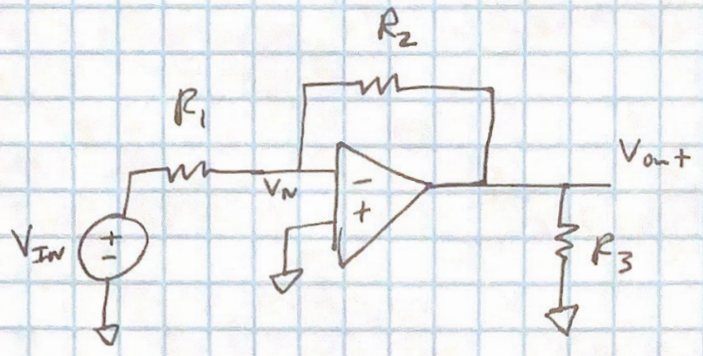
$$4V - (i_2 * 10k\Omega) - 0.7V - (i_2 * 10k\Omega) = 0$$

This should reduce down to $i_2 = \frac{3.3V}{20k\Omega} = 165\mu A$, which gives a 1.65V drop across each resistor. Additionally, this gives a voltage of 2.35V at the anode of the rightmost diode. With the 10V source at the cathode of the middle diode, this would make the voltage across the middle 10kΩ resistor and diode -7.65V, meaning current would be flowing the wrong direction through the diode and confirming the initial assumption that it is off. This gives us the result of $i_2 = 165\mu A$.

9. a)

Case 1: $V_{in} < 0$

Assume D_2 off D_1 on



$$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$$ (inverting amplifier)

$V_N = 0\,V$ (virtual ground due to ideal op amp)

since V_{IN} is negative, V_{OUT} is positive

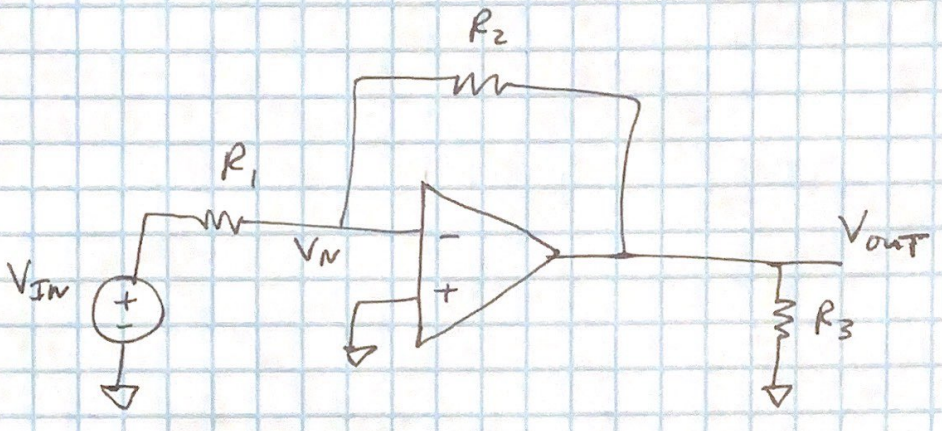
So, D_2 would be reverse biased and D_1 would be forward biased

so assumptions are correct.

current flows out through R_2 and R_3

Case 2: $V_{IN} \geq 0$

Assume D_2 off, D_1 on



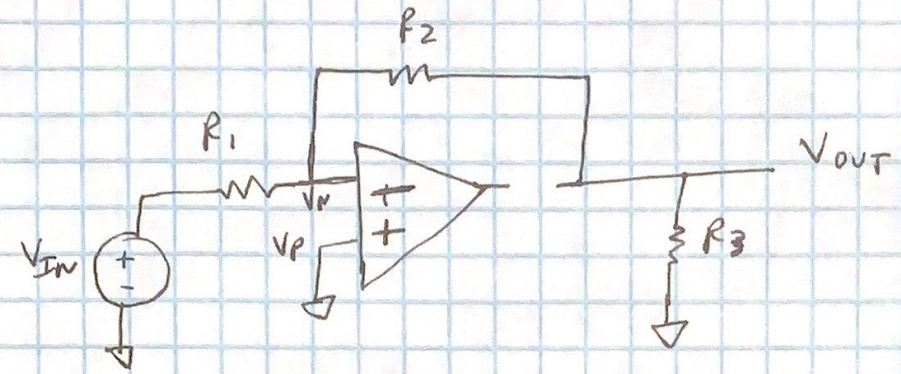
$$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$$

$V_N = 0$ (ideal op amp)

So, current flows into op amp

So, assumption for D_2 is correct but D_1 assumption is wrong

Assume D_1, D_2 both off



op amp has no effect because it is disconnected

So,

$$V_{OUT} = \frac{R_3}{R_1+R_2+R_3} V_{IN}$$

Op amp equation:

$$V_O = A(V_P - V_N) \quad \left(A = \infty \text{ for ideal case}\right)$$

$V_P = 0$

$$V_N = \frac{R_2+R_3}{R_1+R_2+R_3} V_{IN}$$

So, $V_O = -\infty$

↳ V_O of op amp saturates at negative supply

So, $V_{D1} = V_N - \infty \rightarrow$ reverse biased

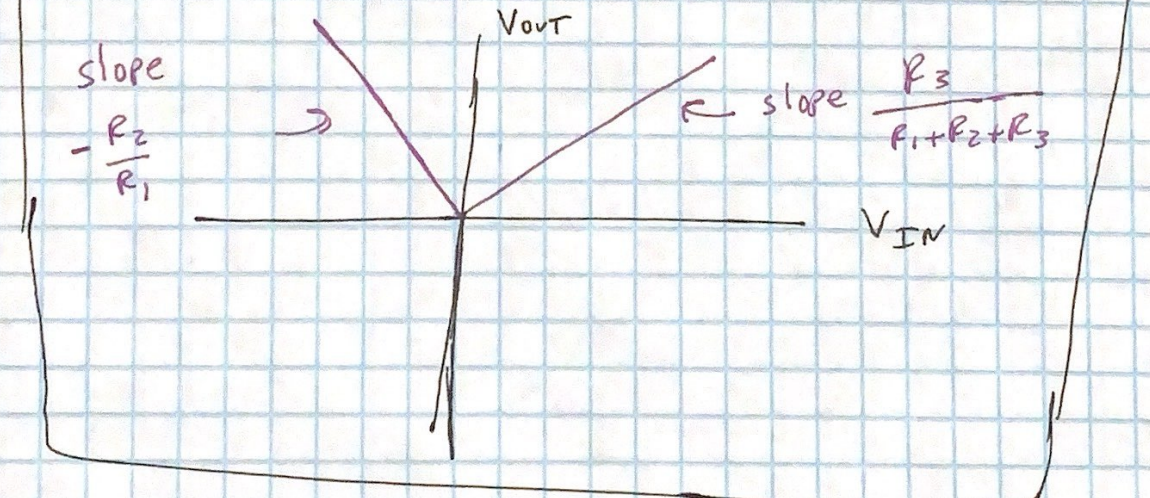
$V_{D2} = -\infty - V_{OUT} = -\infty \rightarrow$ reverse biased

Assumptions are correct

Note, one could make $V_{IN} = 0$ a third case, but when this occurs everything in the circuit goes to 0V so it is modeled by Case 2

So,

$$V_{OUT} = \begin{cases} -\frac{R_2}{R_1} V_{IN}, & V_{IN} < 0 \\ \frac{R_3}{R_1 + R_2 + R_3} V_{IN}, & V_{IN} \geq 0 \end{cases}$$



b) This circuit amplifies the absolute value of the input ~~signal.~~ signal if $\frac{R_2}{R_1} = \frac{R_3}{R_1 + R_2 + R_3}$

Otherwise it still amplifies and rectifies the signal but not the absolute value.

10.

/home/ha1207/ee465_verilog/mux.v - Default

```
`timescale 1ns/1ps
module mux4_1(in0,in1,in2,in3,en,mux_sel,out);          //initiation of module

        input in0,in1,in2,in3,en;                       //initiation of input bits
        input [1:0] mux_sel;                            //initiation of select pin for mux
        output reg out;                                 // initiation of output

        always @(*)begin                                //starts for any change values
        if (en)         begin                           //active low input =1
                        out = 0;                        //active low output
                        end
        else
                        begin
                        case(mux_sel)                   // for selecting a mux pin

                        2'b00 : out = in0;              //assigning values based on select pin
                        2'b01 : out = in1;
                        2'b10 : out = in2;
                        2'b11 : out = in3;
                        endcase

                        end

        end

endmodule
```

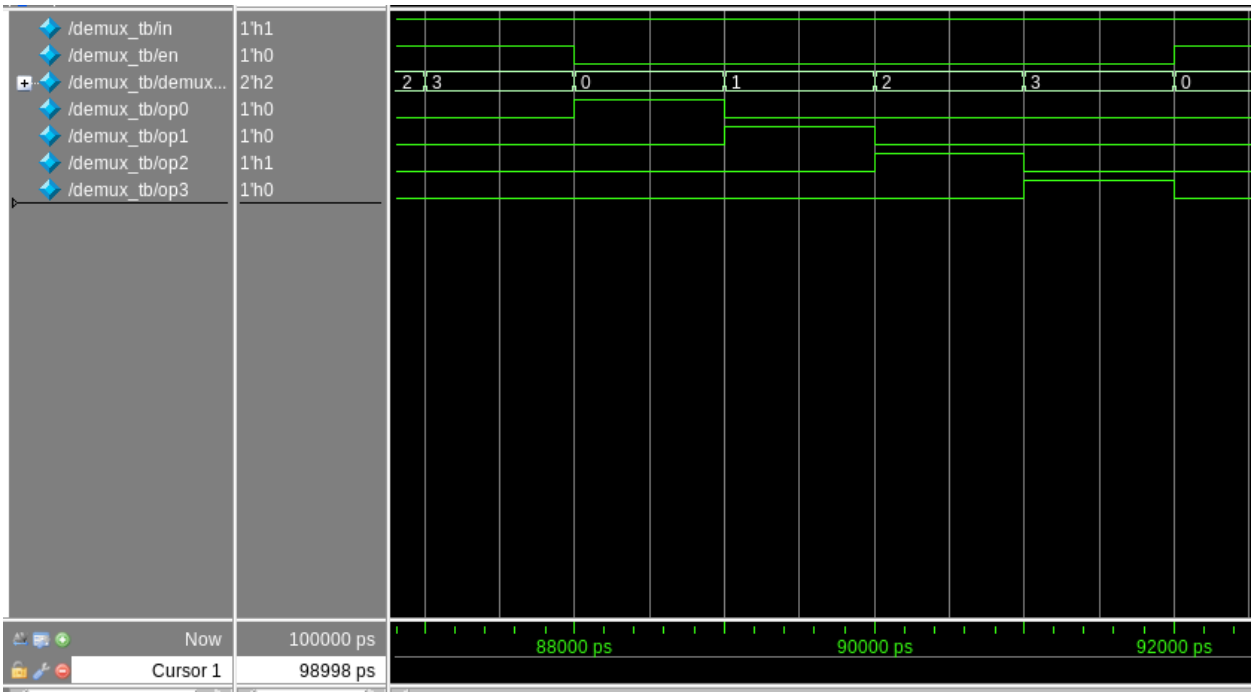
```
`timescale 1ns/1ps
module mux_4_1_tb();

        reg [1:0] mux_sel;                      //inputs are initiated as registers

        reg in0,in1,in2,in3,en;

        wire out;                               //outputs are initiated  as wires

        mux4_1 dut(in0,in1,in2,in3,en,mux_sel,out);     //initiation of dut

                initial in0 = 0;
                initial in1 = 1;
                initial in2 = 0;
                initial in3 = 1;
                initial en = 0;
                initial mux_sel = 2'b00;

                always #1 mux_sel[0] = ~mux_sel[0];
                always #2 mux_sel[1] = ~mux_sel[1];

                always #4 en = ~en;

endmodule
```

```
module demux4_1(in,op0,op1,op2,op3,demux_sel,en);        //initiation of module

        input in,en;                                     //initiation of input pins
        input [1:0] demux_sel;                           //intitiation of select pin for demux output

        output reg op0,op1,op2,op3;                      //initiation of outputs

        always @(*) begin                                // starts for any change in values
                        if (en) begin                    // active low input = 1
                                op0 = 0;
                                op1 = 0;
                                op2 = 0;
                                op3 = 0;
                                end

                        else    begin
                                case(demux_sel)          //for different selections the output is
                                2'b00:begin              // received at a different pin
                                op0 = in;
                                op1 = 0;
                                op2 = 0;
                                op3 = 0;
                                        end
                                2'b01:begin
                                op0 = 0;
                                op1 = in;
                                op2 = 0;
                                op3 = 0;
                                        end
                                2'b10:begin
                                op0 = 0;
                                op1 = 0;
                                op2 = in;
                                op3 = 0;
                                        end
                                2'b11:begin
                                op0 = 0;
                                op1 = 0;
                                op2 = 0;
                                op3 = in;
                                        end


                                endcase
                                end
                end
endmodule
```

/home/ha1207/ee465_verilog/demux_tb.v (/demux_tb) - Default *:

Ln#

```
1   `timescale 1ns/1ps
2
3   module demux_tb();
4
5   reg in, en;                                          //inputs are initiated as registers
6   reg [1:0] demux_sel;
7
8   wire op0,op1,op2,op3;                                //outputs are initiated as wires
9
10          demux4_1 dut(in,op0,op1,op2,op3,demux_sel,en);  //initiation of dut
11                  initial in =1;
12                  initial en =0;
13
14                  initial demux_sel = 2'b00;
15
16                  always #1 demux_sel[0] = ~demux_sel[0]; //toggle the bit 0 every cycle
17                  always #2 demux_sel[1] = ~demux_sel[1]; //toggle the bit 1 every 2 cycles
18
19                  always #4 en = ~en;                  //toggle the enable pin every 4 clock cycles
20
21  endmodule
22
```


/demux_tb/in
/demux_tb/en
/demux_tb/demux...
/demux_tb/op0
/demux_tb/op1
/demux_tb/op2
/demux_tb/op3
1'h1
1'h0
2'h2
1'h0
1'h0
1'h1
1'h0
2
3
0
1
2
3
0
Now
100000 ps
Cursor 1
98998 ps
88000 ps
90000 ps
92000 ps